

**WTN4165**  
**OTP voice musical chip**  
**with MCU**

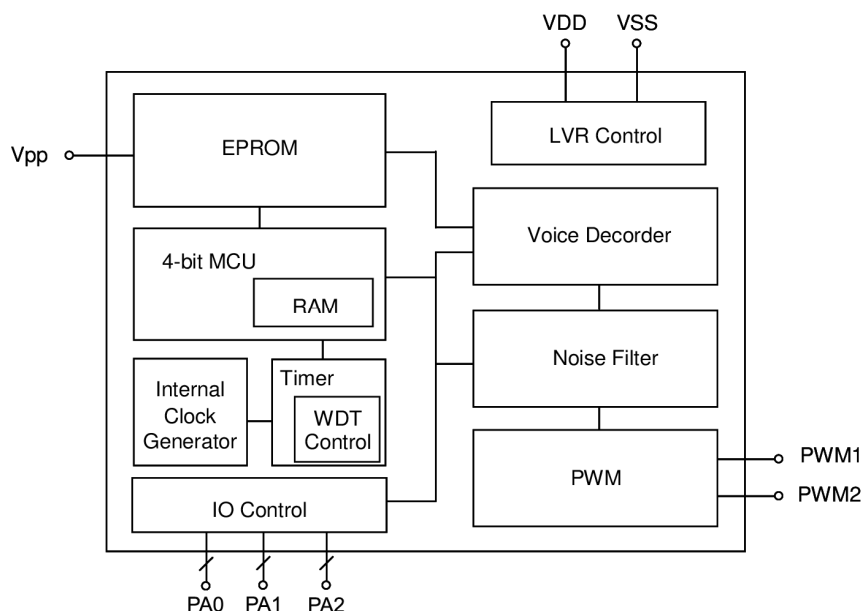
## 1. GENERAL DESCRIPTION

WTN4165 is a powerful 4-bit micro-controller based sound processor. It has embedded OTP (One Time Programmable) EPROM. There is only 1-channel speech with high quality direct-drive PWM output. By using the high fidelity ADPCM speech synthesis algorithm and a built-in noise filter, it can produce outstanding quality voices. Wide range sampling rate up to 44.1kHz is supported. The RISC MCU architecture is very easy to program and control, various applications can be easily implemented. There are 44 instructions, and most of them are executed in single cycle. Furthermore, a HALT mode (sleep mode) is designed to minimize power dissipation. Through +/- 0.5% accurate internal oscillation, external  $R_{osc}$  is unnecessary.

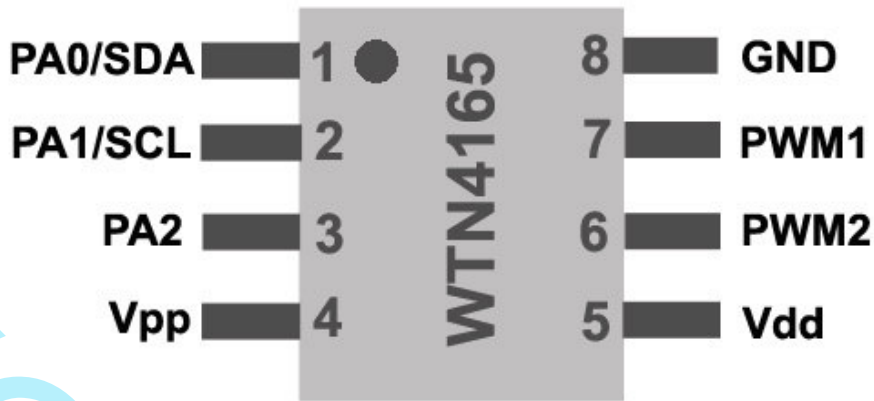
## 2. FEATURES

- Wide operating voltage range: 2.0V to 5.5V.
- 4-bit RISC type micro-controller with 44 instructions.
- ROM Size 400K x 10 bit. 96x4-bit RAM, divided into 2 pages
- 1MHz instruction frequency.
- HALT mode to save power, less than 1uA standby current.
- Precisely embedded oscillator with build-in resistor  $R_{osc}$  (+/- 0.5%).
- Low voltage reset (LVR=1.8V), watch-dog reset and I/O port reset are all supported to protect the system.
- 3 flexible I/Os with optional function: floating, pull-high, strong / weak pull-high, Reset input, IR carrier output. I/O's direction is controlled by registers. For the output port, users can select the normal Drive current output or large Sink current output to directly drive high brightness LED.
- Infrared output: optional IR carrier frequency and optional data high/low IR output supported.
- New high fidelity ADPCM speech synthesis algorithm.
- Built-in noise filter for less background noise at lower volume especially.
- One 9-bit hardware PWM output.
- Support large PWM current output.
- Mute mode speech algorithm to save ROM size.
- A unique fast writing mode is provided to speed up OTP writing time.
- A special ICP (In Circuit Programming) writing function is supported for user to fabricate PCBA in advance.
- Programmable code protection is provided. (When the Security-Bit is burnt down, data can't be read.)

## 3. BLOCK DIAGRAM



#### 4. PAD DESCRIPTION



Pad Name	Pad No.	ATTR.	Description
PA0/SDA	1	I/O	Bit 0 for Port A, or serial data input at programming mode.
PA1/SCL	2	I/O	Bit 1 for Port A, or serial clock input at programming mode.
PA2/IR	3	I/O	Bit 2 for Port A, or IR transmitter pin.
Vpp	4	Power	Positive high power for programming
VDD	5	Power	Positive power.
PWM2 /Mode	6	O	PWM output 2, or select programming mode.
PWM1	7	O	PWM output 1.
GND	8	Power	Negative power.

#### 5. IO PORTS

There are 3 I/O pins at most, designated as PA0~PA3. All the I/O ports can be configured as input or output by registers. For the input port, we provide an internal pull-high register option for convenience. For the output port, users can select the large sink current output or normal drive current output. The PA2 pin can be optioned as an infrared (IR) output pin. An IR port can be large sink current or normal drive current output. The pull-high resistor of all the I/O ports has two kinds of option: weak and strong. The weak one is about 750kΩ @3V for normal application and the strong one is about 33kΩ @3V. When users configure the weak or strong pull-high resistor, the pull-high resistors of all I/O ports are set as the option value.

#### 6. AUDIO SYNTHESIZER

There is 1-ch voice, and all modes are auto-played back by hardware. One audio output stages: 9-bit PWM is supported. The WTN4 series supports 9-bit PCM and encoded ADPCM speech data. Of course, the PCM speech has higher quality and occupies more ROM space than the ADPCM one. Use the encode software to generate the PCM or ADPCM speech data. The voice start address is loading to VPR when executing the PLAY command. There is an option of normal PWM current or large PWM current for different customer demand. The large PWM current consumes more current and makes sound louder. A Noise-Filter is built-in. When users enable this option, hardware will suppress the noise to reduce the background noise automatically. Users can also disable this option up to the sound source. A voice channel includes a PFLG, a VPR, a voice decoder, a QIO control code generator and an 8-bit sample rate timer (TM) whose timer clock source (TCS) is fixed to 1MHz. It supports PCM and encoded ADPCM speech data. The WTN4 series supports another special mute mode for speech. When a speech like the vocal or talk has a lot of suspension or silence, using the mute mode saves much ROM space. Turn on the mute mode option of the encode software to save your cost.

## 7. ELECTRICAL CHARACTERISTICS

### 7.1. Absolute Maximum Rating

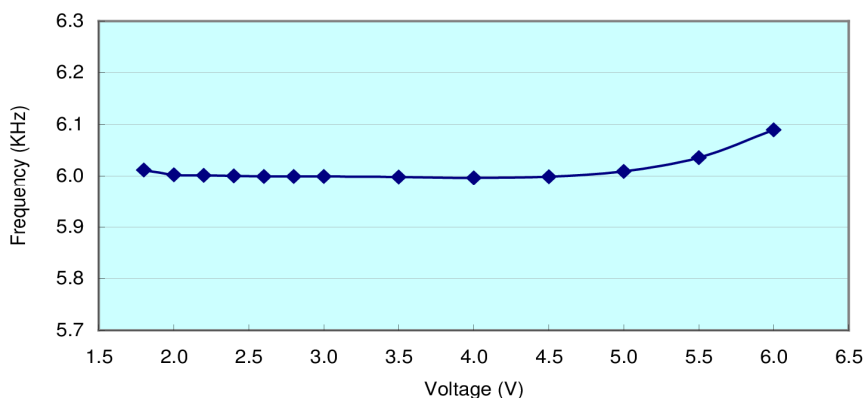
Symbol	Rating	Unit
VDD~GND	-0.5 ~ +6.0	V
V <sub>in</sub>	GND-0.3 < V <sub>in</sub> < VDD+0.3	V
T <sub>op</sub> (operating)	-20 ~ +70	°C
T <sub>st</sub> (storage)	-25 ~ +85	°C

### 7.2. DC CHARACTERISTICS

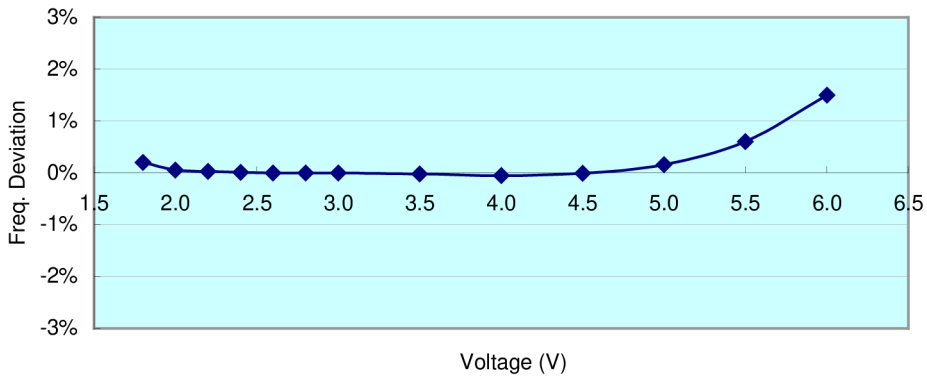
Symbol	Parameter	VDD	Min.	Typ.	Max.	Unit	Condition
VDD	Operating voltage		2.0	3	5.5	V	1 MHz
I <sub>sb</sub>	Supply current	Halt mode	3	0.1	0.5	uA	Sleep, no load
			4.5	0.1	0.5		
I <sub>op</sub>	Operating mode	3		3.3		mA	1MHz, no loading
		4.5		5.3			
I <sub>il</sub>	Input current (Internal pull-high)	Weak (750k ohms)	3	-3.7		uA	V <sub>il</sub> =0v
			4.5	-10			
		Strong (33k ohms)	3	-67			
			4.5	-170			
I <sub>oh</sub>	Output high current	3		-7		mA	V <sub>oh</sub> =2.0V
		4.5		-11			V <sub>oh</sub> =3.5V
I <sub>ol</sub>	Output low current (Large current)	3		17		mA	V <sub>ol</sub> =1.0V
		4.5		26			V <sub>ol</sub> =1.0V
I <sub>PWM</sub>	PWM output current (Normal)	3		60		mA	Load=8 ohms
		4.5		100			
I <sub>PWM</sub>	PWM output current (Large)	3		70		mA	Load=8 ohms
		4.5		117			
ΔF/F	Frequency deviation by voltage drop (1MHz)	3		0.1		%	Fosc(3.0v) - Fosc(2.4v)
							Fosc(3v)
		4.5		-0.1			Fosc(4.5v) - Fosc(3.0v)
						Fosc(4.5v)	
ΔF/F	Frequency lot deviation (1MHz)	3	-0.5		0.5	%	F <sub>MAX</sub> (3.0v) - F <sub>TYP</sub> (3.0v) F <sub>MAX</sub> (3.0v)
Fosc	Oscillation Frequency	-	0.97	1	1.03	MHz	VDD=2.0~5.5V

### 7.3. VOLTAGE vs. FREQUENCY

Voltage vs Frequency (6.0KHz@3V)

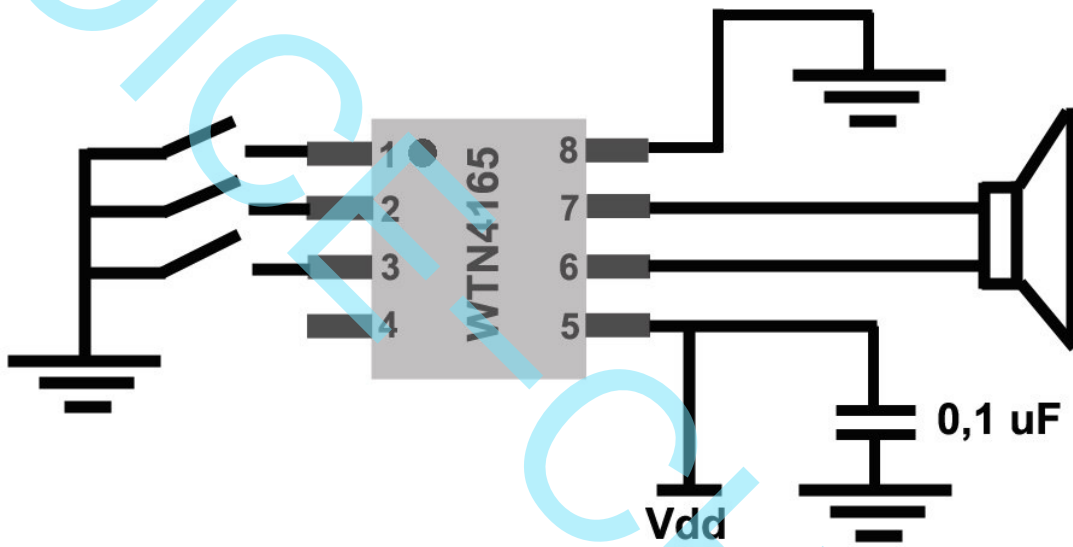


Voltage vs Freq. Deviation (6.0KHz@3V)

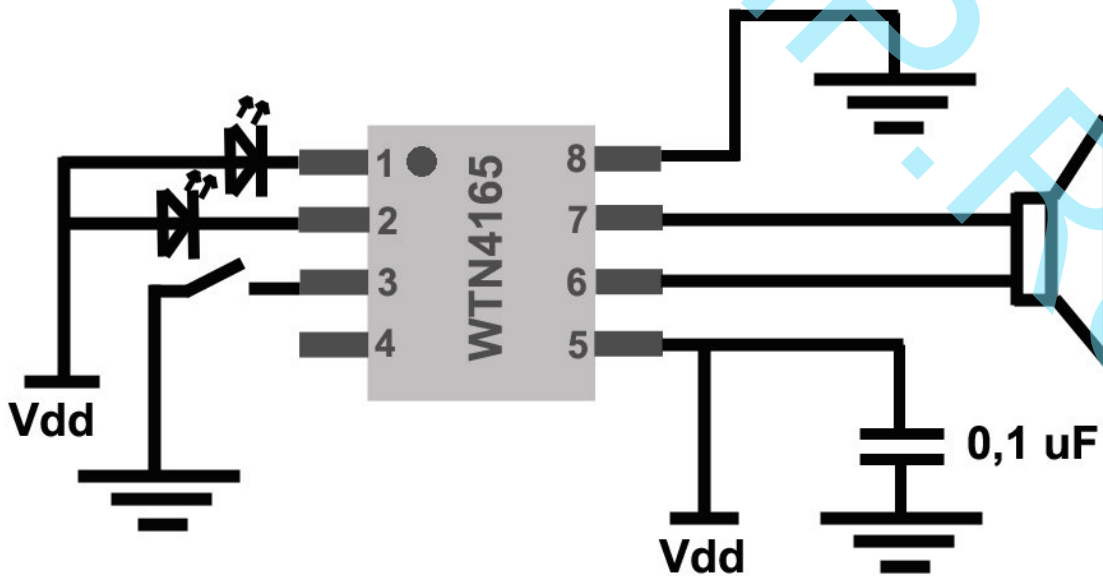


## 8. TYPICAL APPLICATION CURCUITS

### 8.1. Simple three push button application.

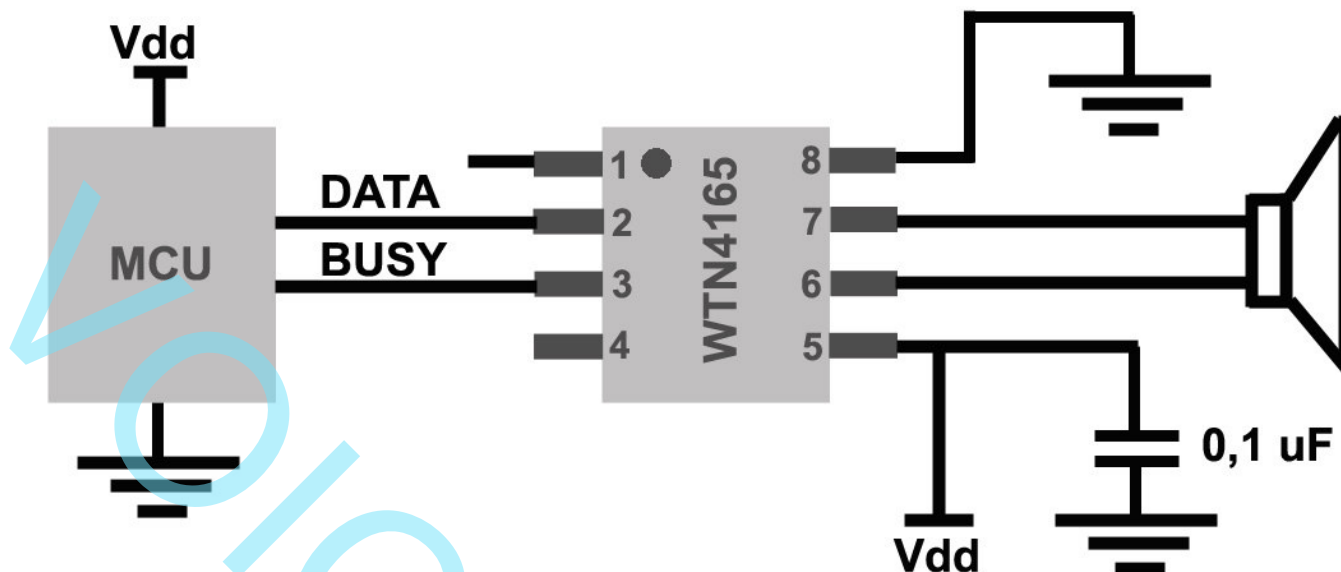


### 8.2. Simple push button + two LEDs appliacion.



### 8.3. One-line serial communication.

In one-line serial port mode, can use MCU to control and send data to WTN4 chips through DATA line to realize the functions of controlling voice play, loop playback, stop playing.



*Note: when the power supply of WTN4 series voice chip is connected to 3.3V, the IO port is 3.3V level; while connected to 5V, IO port will be 5V level. When there is different power supply between single-chip microcomputer and WTN4 series voice chip, it is required to add the level switching circuit. When it is one line control, pin PA1 is the data input pin. When it is two line control, pin PA1 is the clock input pin. When wiring, capacitor C1 of VDD end should try to close to the VDD pin, in order to enhance the anti-interference ability of WTN4 voice chips.*

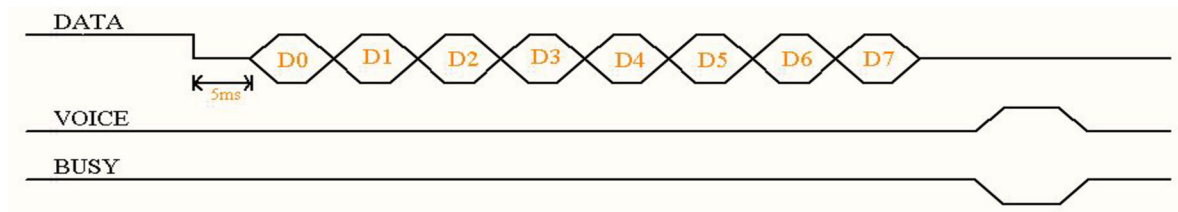
One-line audio corresponding addresses:

Data(hexadecimal)	Number of playing audio
00H	Play zero audio
01H	Play the 1st audio
02H	Play the 1st audio
.....	.....
ECH	Play the 236th audio
EDH	Play the 237th audio
EEH	Play the 238th audio
EFH	Play the 239th audio

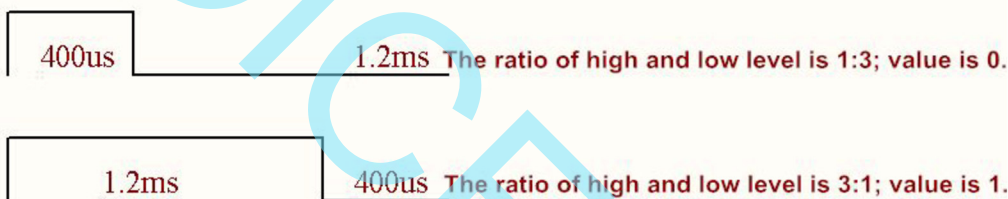
One-line audio and command code:

Command code	Function	Description
F2H	Repeat playing current audio	This command can make loop play of the current audio, can be sent when it plays or stops.
FEH	Stop playing current audio	This command can stop playing the current audio.

One-line serial command sequence diagram:



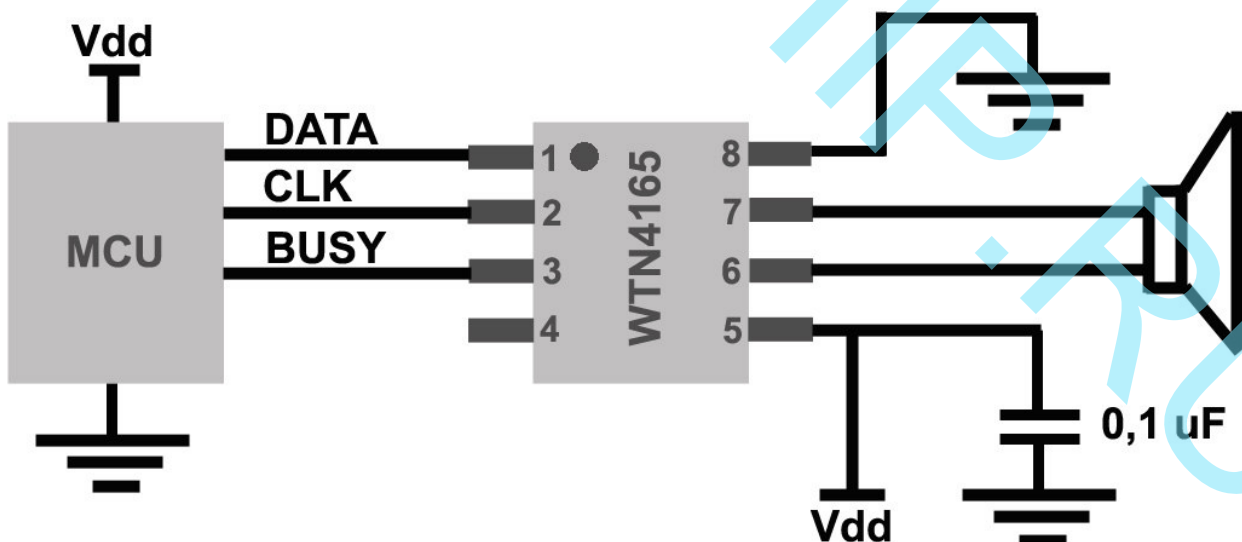
One-line serial port controls time sequence only via one data communication line. According to the duty ratio of electric level, different duty ratios represent different data bits. Pull data signal down 5 ms first, and then sending data. The data duty ratio of high level and low level is 1:3; that represents data bit is 0. When data duty ratio of high level and low level is 3:1, that represents data bits is 1. High level in the front, low level at the back. For the data, low bit sent first, then send high bit. D0 ~ D7 mean one address or command data; the data of 00 h ~ EFH is address instruction; F2H is the command for loop playback of current audio; FEH is the command to stop the current voice play.



Note: BUSY is busy signal output. After sending data successfully, 250us later, BUSY output will response; BUSY output 25ms later, voice output will response. CLK pull-down time range: 4ms~40ms, recommended to use 5ms. Timing range of one-line high and low level 1:3 is 350us:1.05ms ~1.2ms:3.6ms, recommended to use 400us:1.2ms.

#### 8.4. Two-line serial communication.

Two-line serial port mode is composed of two communication lines, that are data line and clock line. Through MCU, use two-line communication to control WTN4 chips to realize the functions of controlling voice play, loop playback, stop playing.



Note: when the power supply of WTN4 series voice chip is connected to 3.3V, the IO port is 3.3V level; while connected to 5V, IO port will be 5V level. When there is different power supply between single-chip microcomputer and WTN4 series voice chip, it is required to add the level switching circuit. When it is one line control, pin PA1 is the data input pin. When it is two line control, pin PA1 is the clock input pin. When wiring, capacitor C1 of VDD end should try to close to the VDD pin, in order to enhance the anti-interference ability of WTN4 voice chips.

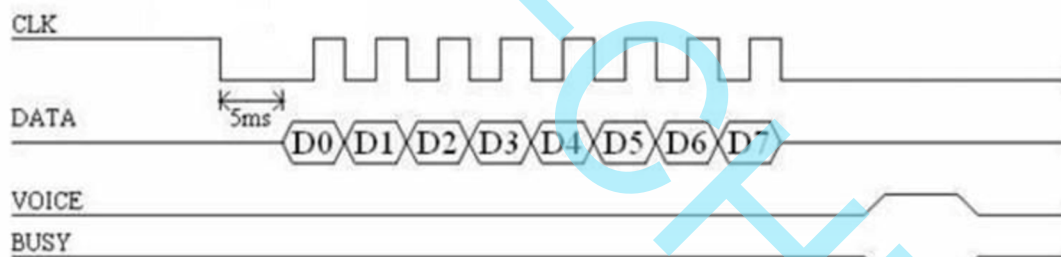
Two-line audio corresponding addresses:

Data(hexadecimal)	Number of playing audio
00H	Play zero audio
01H	Play the 1st audio
02H	Play the 1st audio
.....	.....
ECH	Play the 236th audio
EDH	Play the 237th audio
EEH	Play the 238th audio
EFH	Play the 239th audio

Two-line audio and command code:

Command code	Function	Description
F2H	Repeat playing current audio	This command can make loop play of the current audio, can be sent when it plays or stops.
FEH	Stop playing current audio	This command can stop playing the current audio.

Two-line serial command sequence diagram:



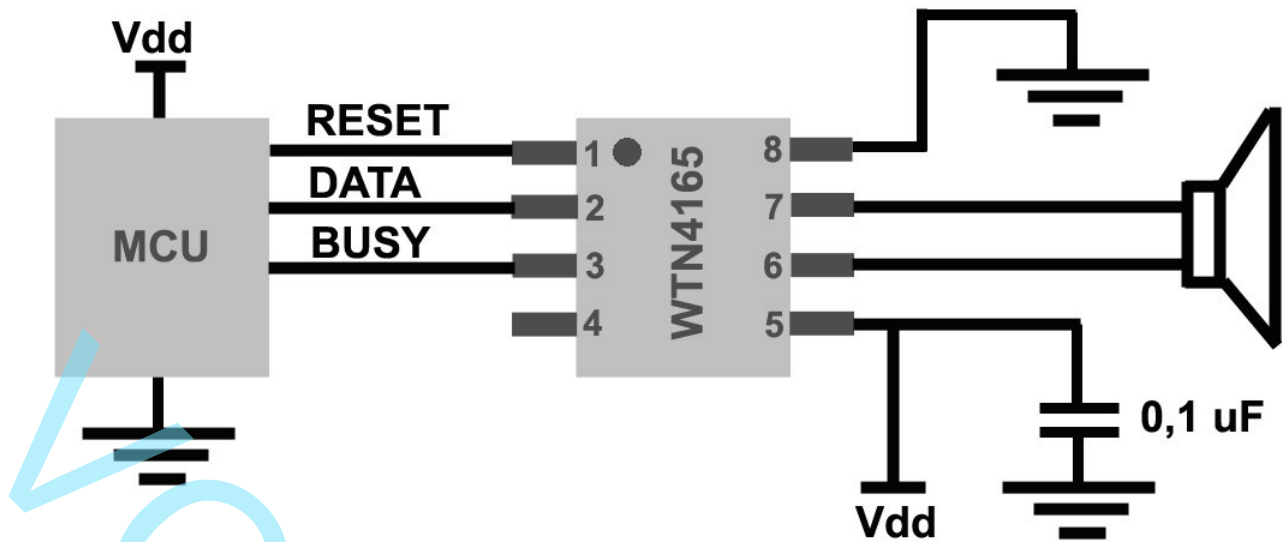
Two-line serial port control mode is composed of CLK and DATA pin. Each time send one byte of data, CLK signal pull down 4ms-40ms, recommended to sue 5ms to wake up WTN4 voice chips. Receive low data first, in the rising edge of clock. Clock cycle is 320us~1.5ms, recommended to use 400us. For the data, low bit sent first, then send high bit. D0 ~ D7 mean one address or command data; the data of 00H ~ EFH is address instruction; F2H is the command for loop playback of current audio; FEH is the command to stop the current voice play.

*Note: CLK pull-down time range: 4ms~40ms, recommended to use 5ms. High level time range of CLK cycle is 150us~4ms; low level time range of CLK cycle is 150us~4ms, recommended to use the time of CLK high and low level 200us.*

### 8.5. Pulse number control mode.

Pulse number control mode is send different number of pulse on DATA line to control audio address play. This control mode has less ports, can control many audio addresses. Usually used in the applications of less MCU control port.



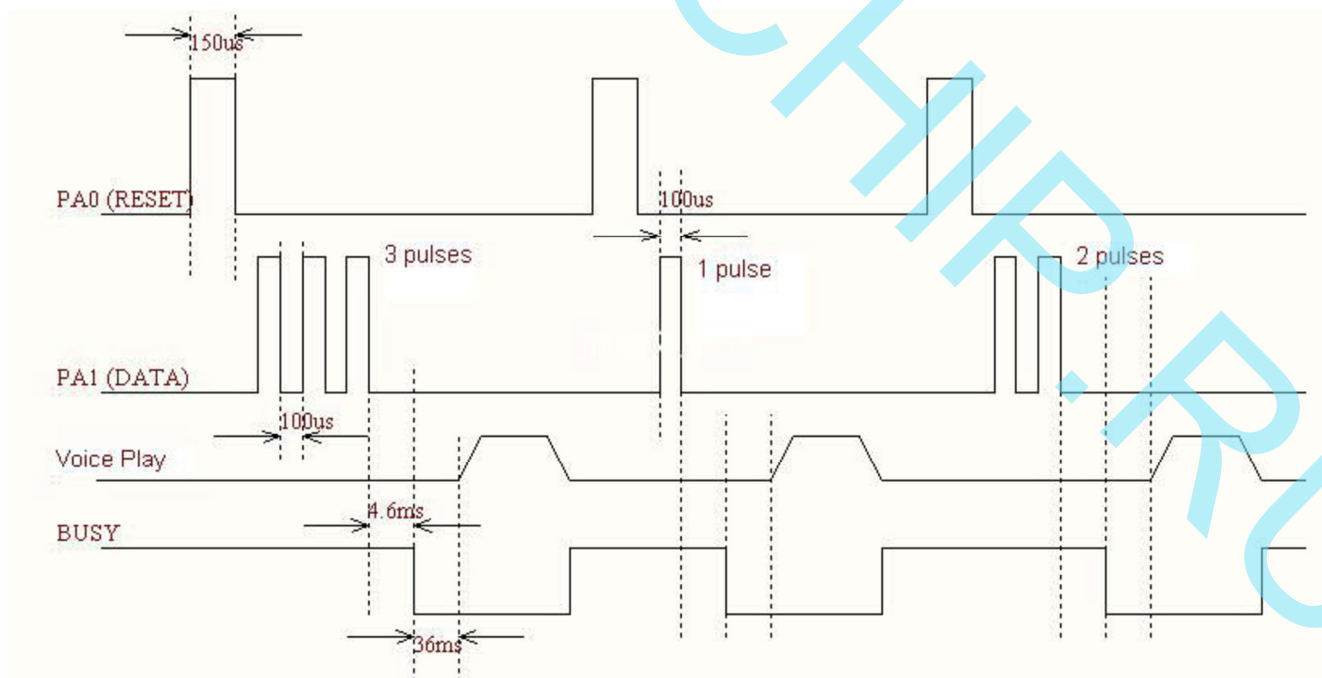


Note: when the power supply of WTN4 series voice chip is connected to 3.3V, the IO port is 3.3V level; while connected to 5V, IO port will be 5V level. When there is different power supply between single-chip microcomputer and WTN4 series voice chip, it is required to add the level switching circuit. When it is one line control, pin PA1 is the data input pin. When it is two line control, pin PA1 is the clock input pin. When wiring, capacitor C1 of VDD end should try to close to the VDD pin, in order to enhance the anti-interference ability of WTN4 voice chips.

Pulse number mode audio corresponding addresses:

Number	Pulse	Audio address
1	1	1
2	2	2
3	3	3
.....	.....	.....
238	238	238
239	239	239

Pulse number control sequence diagram:

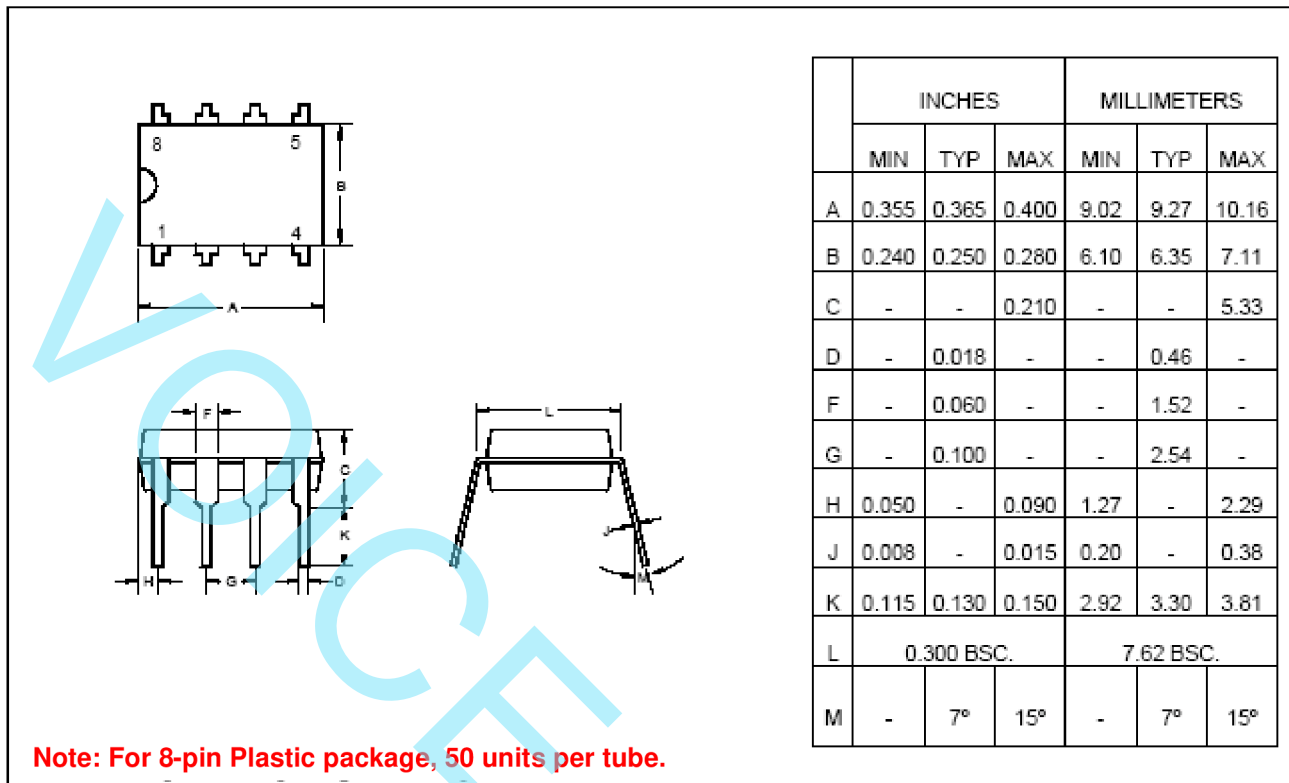


In pulse control timing, first pull up RESET signal 150us, and then send DATA. The pulse in DATA needs to maintain a high level of 100US, and the interval time between the two pulses need 100us. After sending pulse data, 4.6ms later, BUSY signal will output. BUSY output 36ms later, it starts playing the address speech. BUSY will also change as voice playback ends.

Note: time range of pulse signal high level width: 50us~2ms, recommended to use 100US; interval time range of pulse signal: 100us~4ms, recommended to use 100us. The high level range of the reset signal is greater than 100US, recommended to use 150us.

## 9. PACKAGE DIMENSIONS

### 8-Pin Plastic DIP (300 mil)



### 8-Pin Plastic SOP (150 mil)

